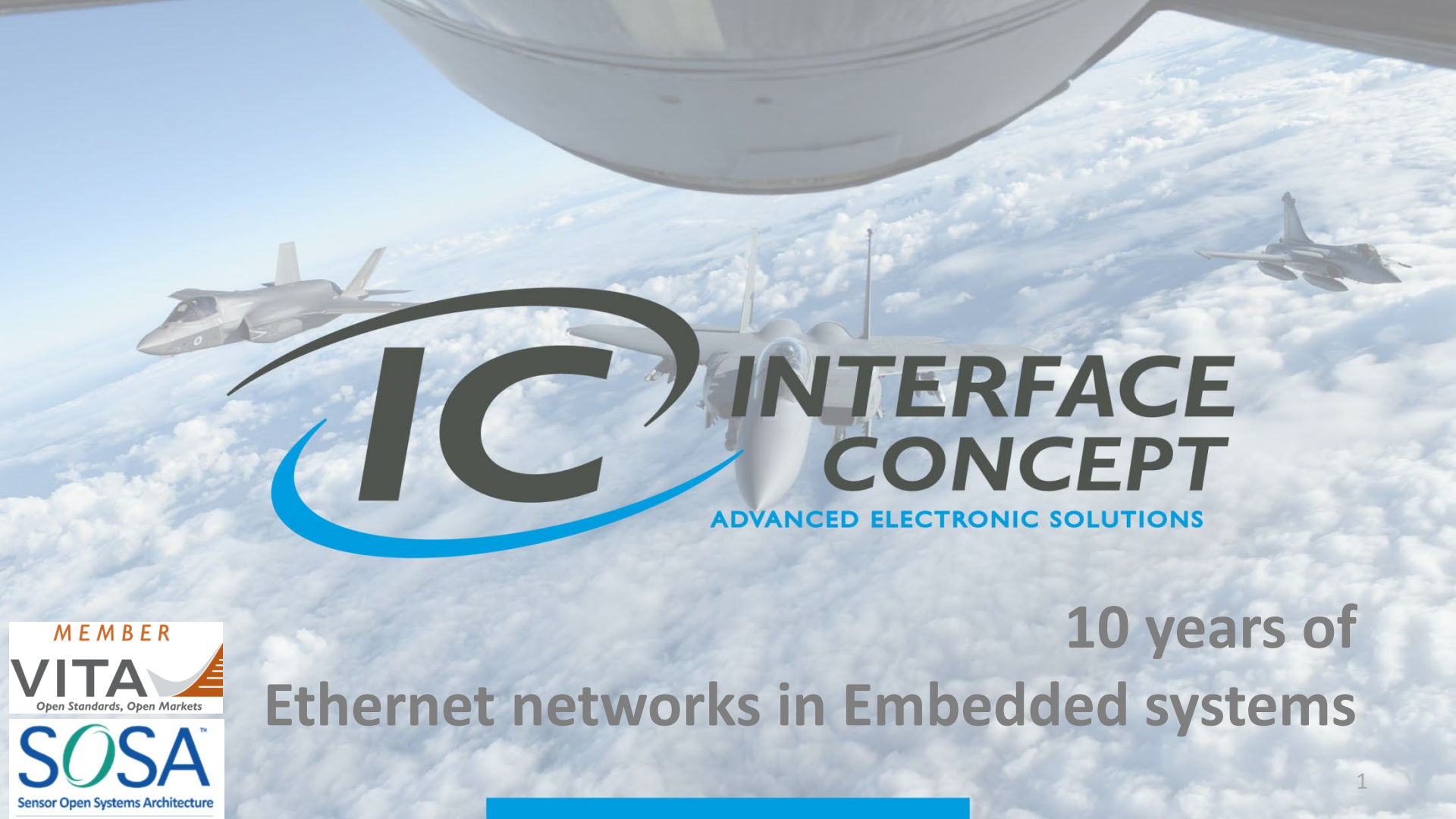


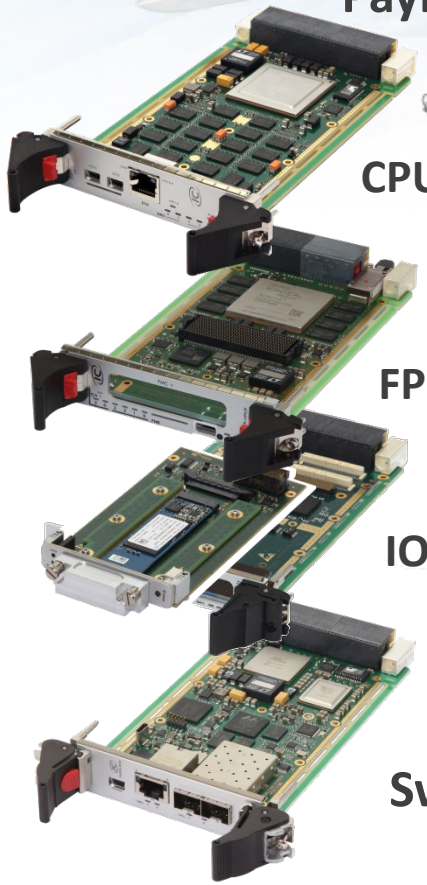
MEMBER
VITA
Open Standards, Open Markets

SOSA™
Sensor Open Systems Architecture

10 years of Ethernet networks in Embedded systems

Embedded Systems

Payload Boards



CPU

FPGA

IOs

Switch

VITA 48

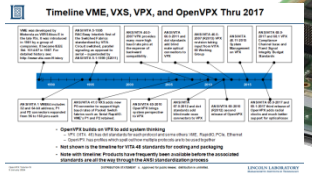
cooling schemes

Air Cooled

Conduction Cooled

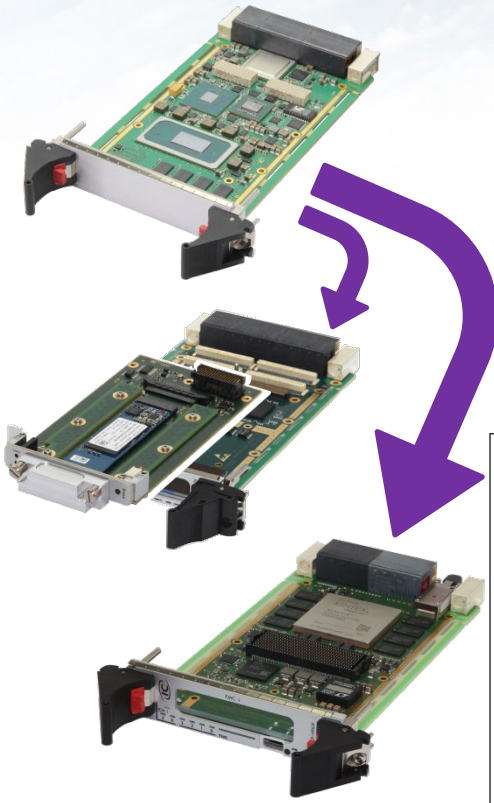
Air Flow Through

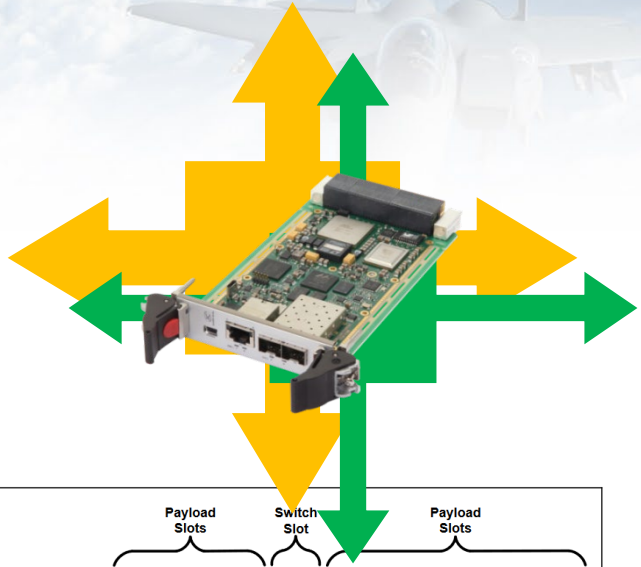
Control Flow / Data Flows

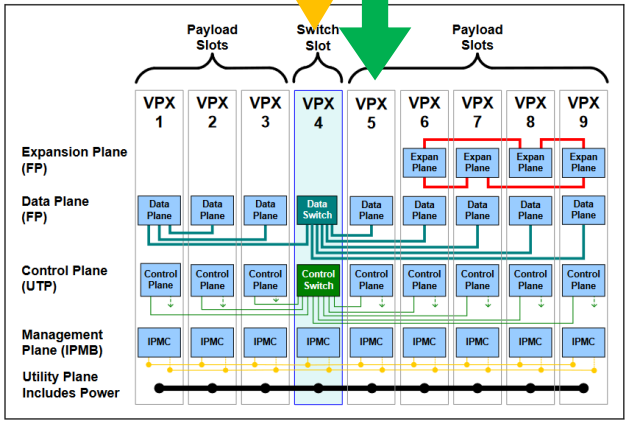


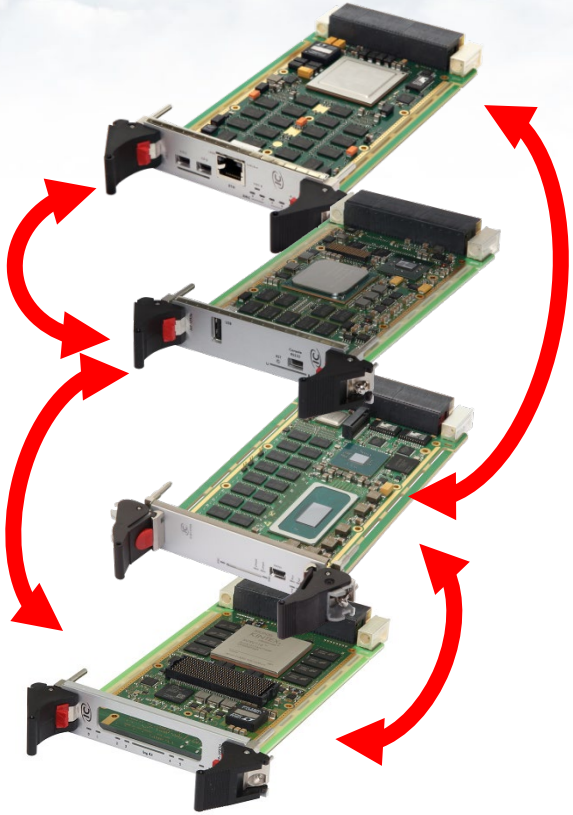
Refer to OpenVPX Tutorial and Common Practices
G. Rocco
Timeline VME, VXS, VPX, and OpenVPX Thru 2017

Control Flow / Data Flows





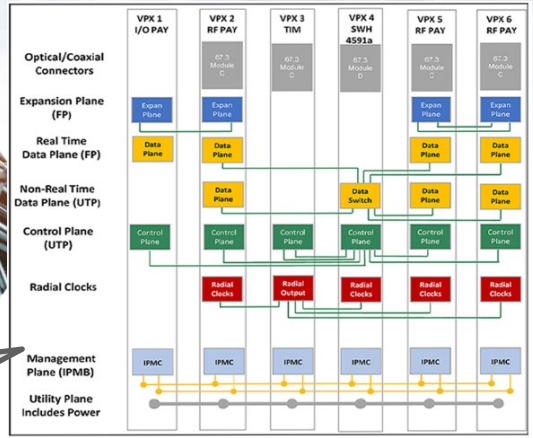


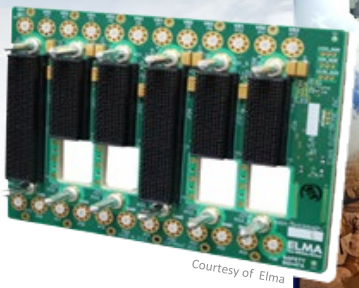


VITA 65.0 Slots & Backplane profiles

OpenVPX™

VITA 65.0 Backplane Profile





Courtesy of Elma

VITA 65.0 Slot Profile

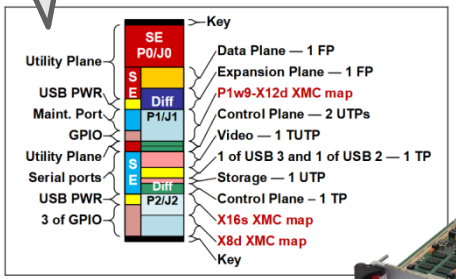


Figure 14.2.16-1 SLT3-PAY-1F1F2U1TU1T1U1T-14.

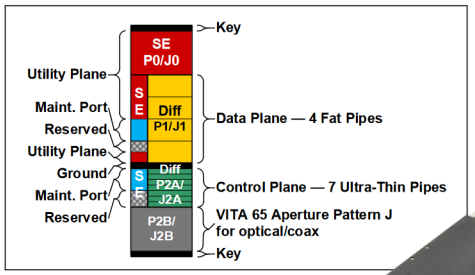


Figure 14.8.7-1 SLT3-SWH-4F1U7U1J-14.8.7-

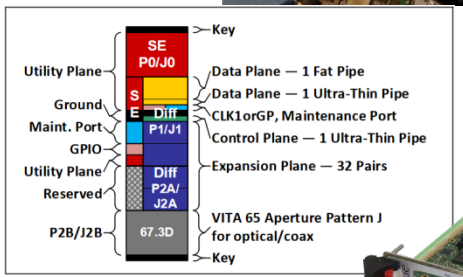
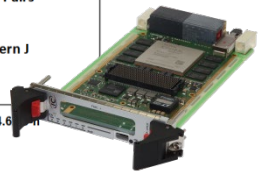


Figure 14.6.13-1 SLT3-PAY-1F1U1S1S1U1U4F1J-14.6



VITA 65.1 Module profiles

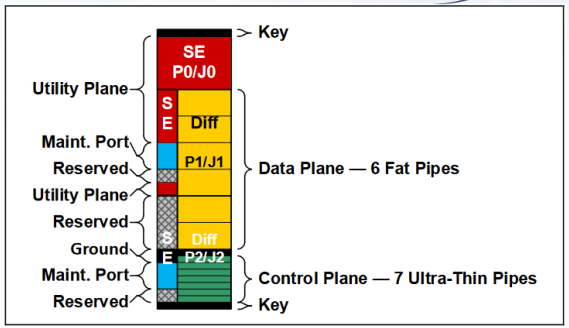
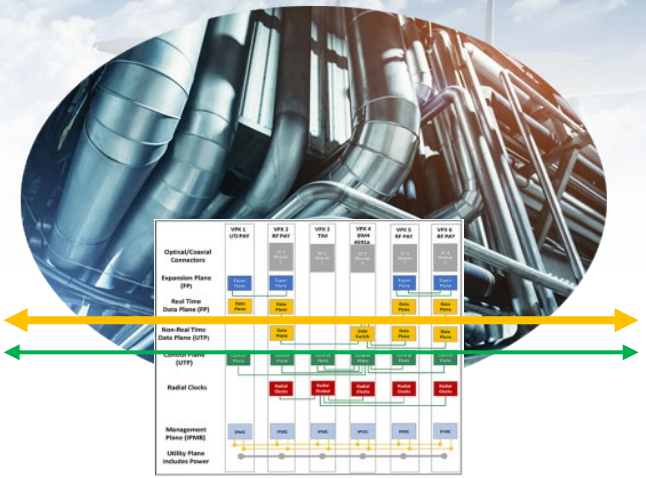


Figure 14.4.14-1 SLT3-SWH-6F1U7U-14.4.14



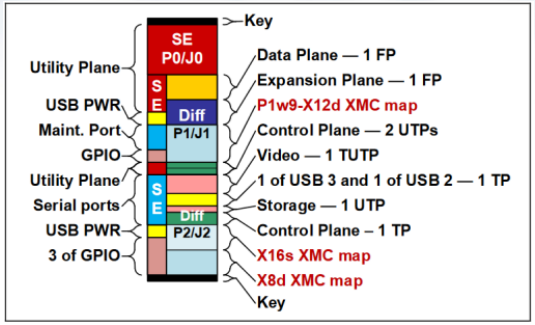


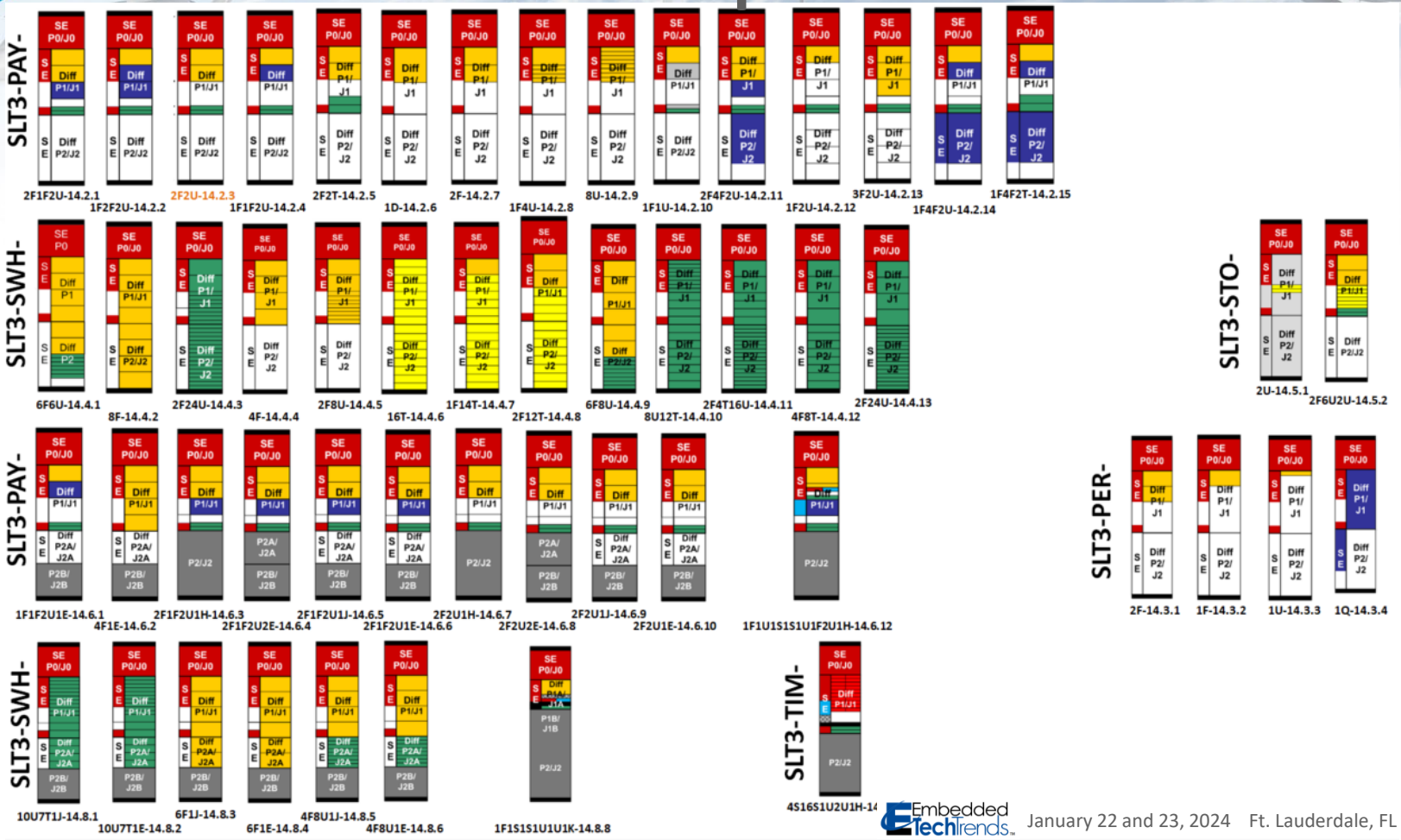
Figure 14.2.16-1 SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16

MOD3-SWH-6F1U7U-16.4.15-			DP01 - DP04, DS01 (FP)	DP05	CPutp01 - CPutp06	CSutp01
MOD3-SWH-6F1U7U-16.4.15- 1	2017-05	SLT3-SWH-6F1U7U-14.4.14	10GBASE-KX4 -- 5.1.5	As 4 UTPs: 1000BASE-KX -- 5.1.2	1000BASE-KX -- 5.1.2	1000BASE-KX -- 5.1.2
MOD3-SWH-6F1U7U-16.4.15- 2	2019-11	SLT3-SWH-6F1U7U-14.4.14	10GBASE-KR -- 5.1.7, 40GBASE-KR4 -- 5.1.8	10GBASE-KR -- 5.1.7, 40GBASE-KR4 -- 5.1.8	10GBASE-KR -- 5.1.7	10GBASE-KR -- 5.1.7
MODA3-16.4.15-	**STD Date**	**Slot Profile**	**Protocols for Copper Planes**			
MODA3-16.4.15- 1	2021-10	SLT3-SWH-6F1U7U-14.4.14	(FPs of DP01 - DP05, DS01	UTPs of DP01 - DP05, DS01)	(CPutp01 - CPutp06, CSutp01)	

VITA 65.1 Module Profile

MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15-			DP01 (FP)		EP00 - EP03	CPutp01, CPutp02	CPtp01
MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15- 1	2019-11	SLT3-PAY-1F1F2U1TU1T1U1T-14.2.1	PCIe Gen 2 -- 5.3.3.2		PCIe Gen 2 -- 5.3.3.2	1000BASE-KX -- 5.1.2	1000BASE-T -- 5.1.3
MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15- 2	2019-11	SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16	PCIe Gen 3 -- 5.3.3.3		PCIe Gen 3 -- 5.3.3.3	10GBASE-KR -- 5.1.7	1000BASE-T -- 5.1.3
MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15- 3	2019-11	SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16	10GBASE-KX4 -- 5.1.5		PCIe Gen 2 -- 5.3.3.2	1000BASE-KX -- 5.1.2	1000BASE-T -- 5.1.3
MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15- 4	2019-11	SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16	40GBASE-KR4 -- 5.1.8		PCIe Gen 3 -- 5.3.3.3	10GBASE-KR -- 5.1.7	1000BASE-T -- 5.1.3

VITA 65 Slots profiles



Additional SOSA Slots profiles

SLT3-PAY-

SLT3-SWH-

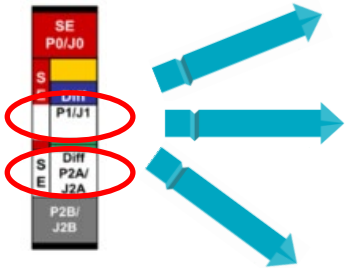
SLT3-PAY-

SLT3-SWH-

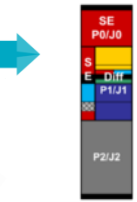
SLT3-TIM-

SOSA™
Sensor Open Systems Architecture
MEMBER

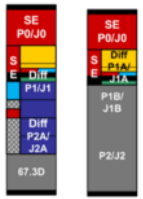
The SOSA Consortium strives to develop an ecosystem that allows interoperability, reuse, and faster delivery of products to market through vertical integration from cables, mechanical interfaces, hardware, software, and system designs



Avoid user defined pins that will subsequently limit interoperability



1F1U1S1S1U1U2F1H-14.6.11



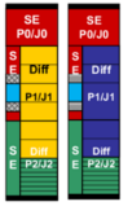
1F1U1S1S1U1U4F1J-14.6.13
1F1U1S1S1U1U1K-14.6.14

4F1U7U1J-14.8.7

1F1U1S1S1U1K-14.8.9

2S1U

6F1U7U-14.4.14

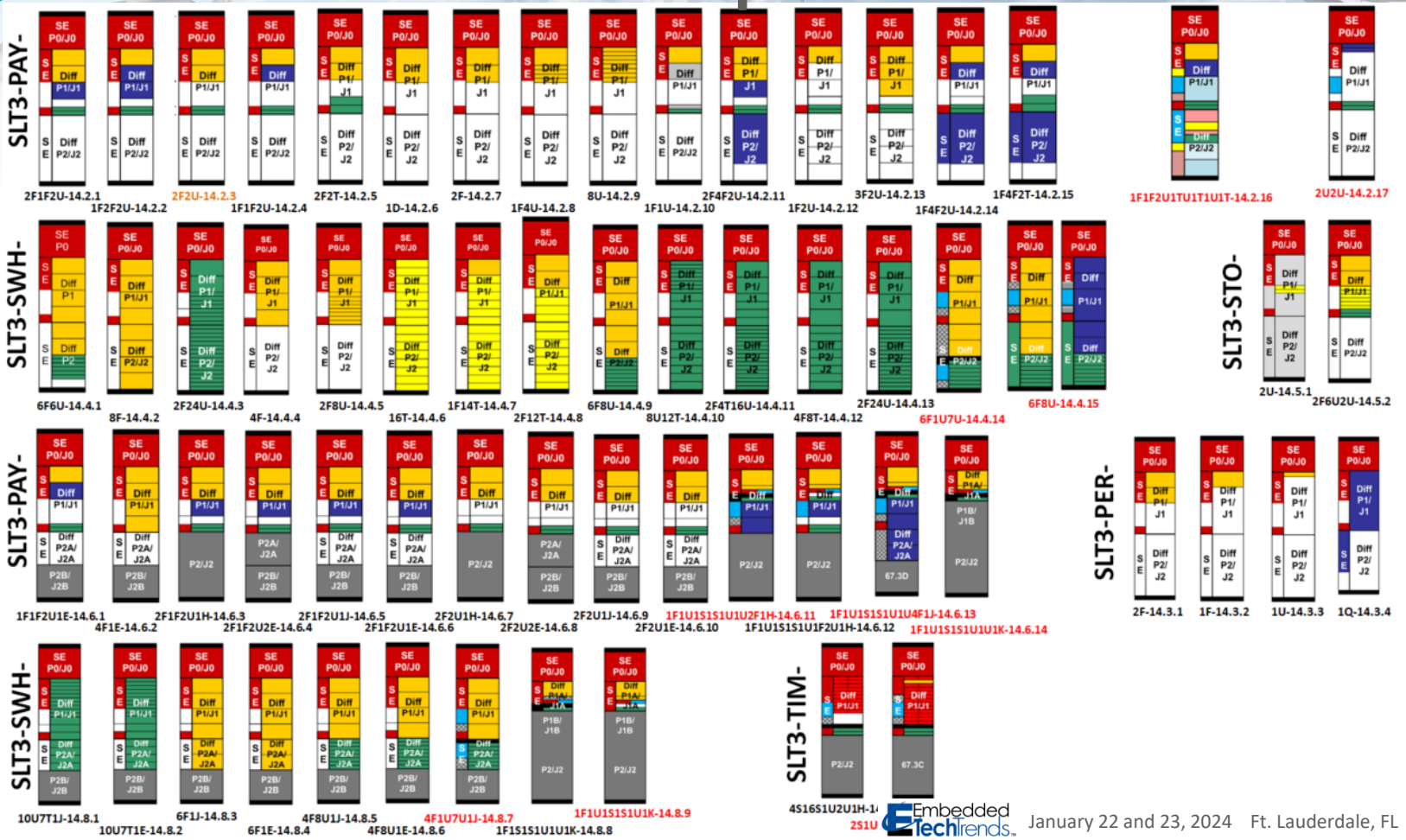


6F8U-14.4.15

1F1F2U1TU1T1U1T-14.2.16

2U2U-14.2.17

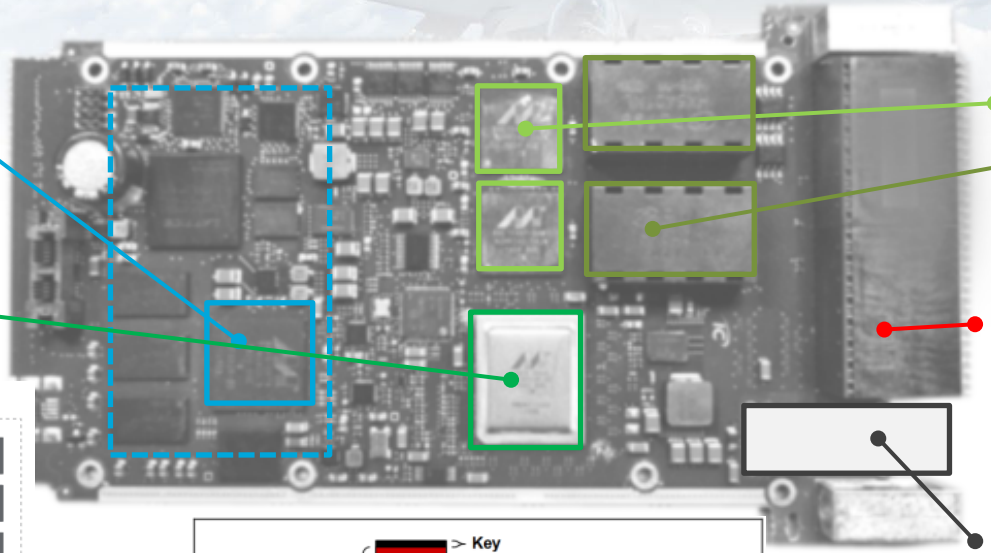
VITA 65 Slots profiles



Architecture of an Ethernet Switch

Mngt Unit supporting the software and management of some Layer3/4 functions

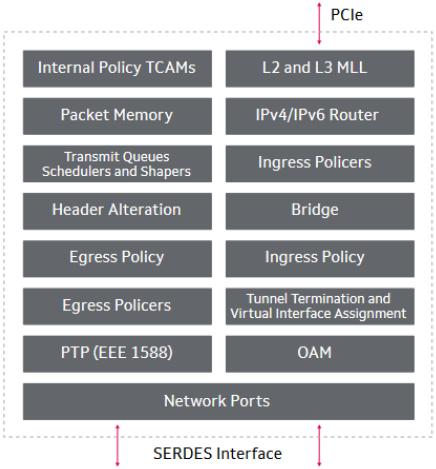
The Ethernet Matrix an highly-integrated packet processors.



1000Base-T and 10GBase-T interfaces require Physical Transceivers and Transformers

Base-KX, -KR, -KR4 electrical interfaces are managed directly by the Switch SerDes

Optical ports
(1000Base-SX, 10GBase-SR, 25GBase-SR, 40GBase-SR4 100GBase-SR4 …)
require optical transceivers



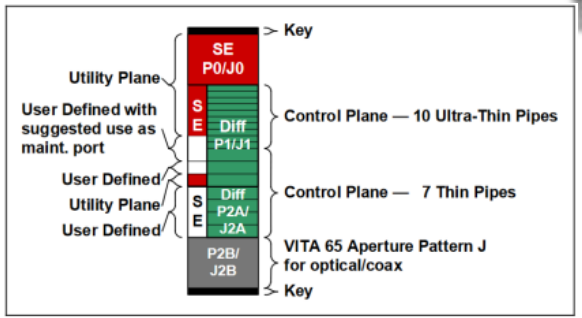
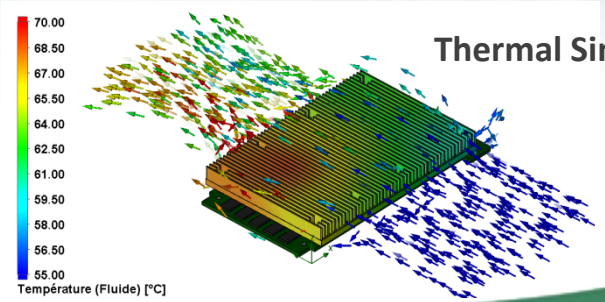


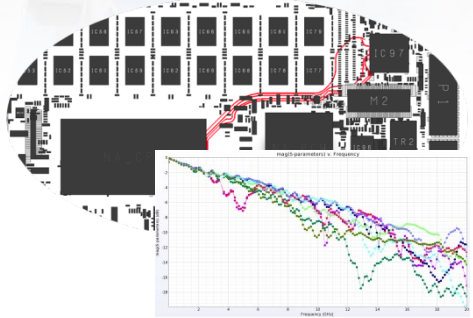
Figure 14.8.1-1 SLT3-SWH-10U7T1J-14.8.1-n

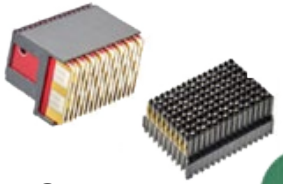
10 years of incredible technological developments



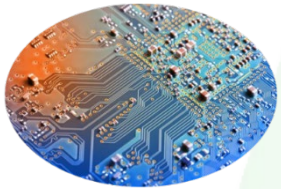
Thermal Simulation

Signal Analysis

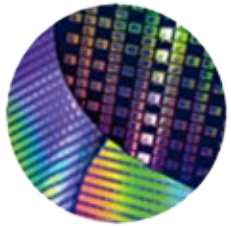




Connectors



PCB Materials



Foundry Process Technologies

72 x 25G + 2 x 10G
45 x 45 mm
1.86 Tbps

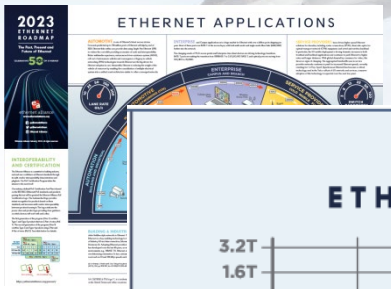
32 x 25/50G
29 x 29 mm
600/1200 Gbps

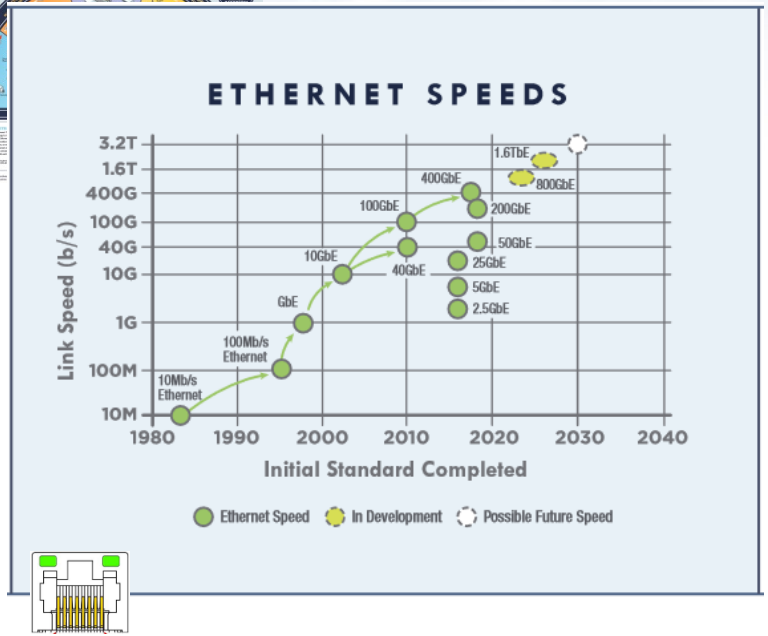
32 x 25 + 1 x 10G
33 x 33 mm
610 Gbps

32 + 1 x 10G
24 x 20 mm
320 Gbps

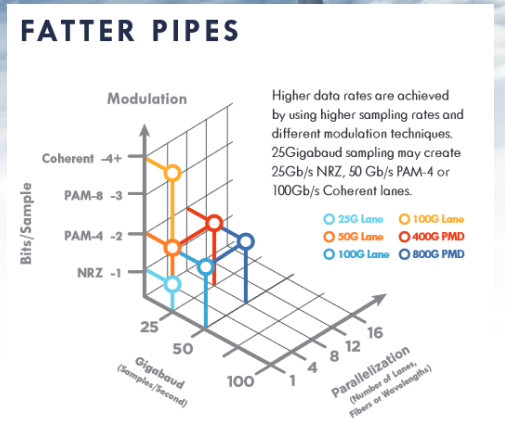
24 + 1G
37.5 x 37.5 mm
24 Gbps

Ethernet Roadmap

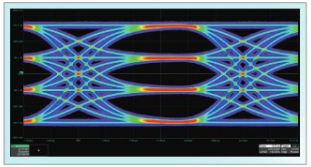




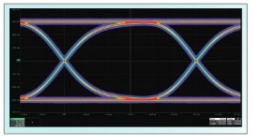
Refer *Ethernet Alliance* Roadmap
https://ethernetalliance.org/technology/ethernet-roadmap/



SIGNALING METHODS

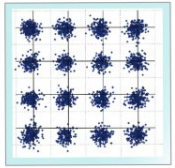


PAM-4

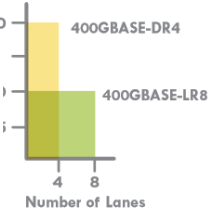


NRZ

Signaling for higher lane rates has transitioned from non-return-to-zero (NRZ) used for 25Gb/s per lane to four level Pulse-amplitude modulation (PAM-4) for 50 Gb/s per lane and above. Coherent Modulation uses more complex modulations for 100Gb/s per lane and above.

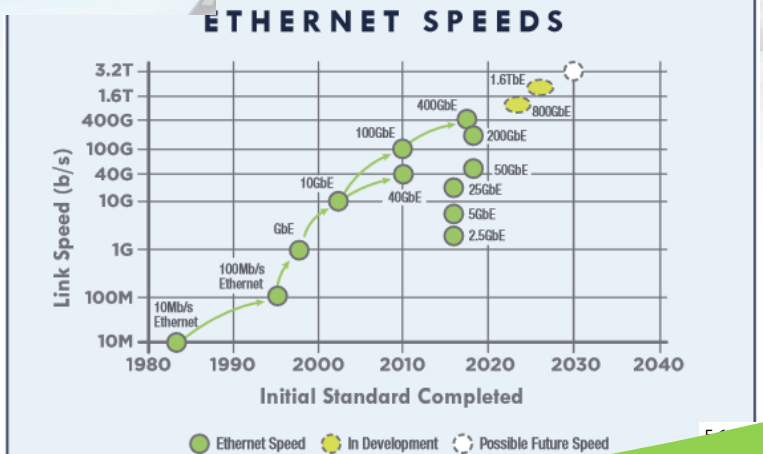


Coherent



After the data rate/lane is chosen, the number of lanes in a link determines the speed. This chart shows how 4 or 8 lanes can be used to generate 400GbE links.

Ethernet protocols in VITA 65



2010

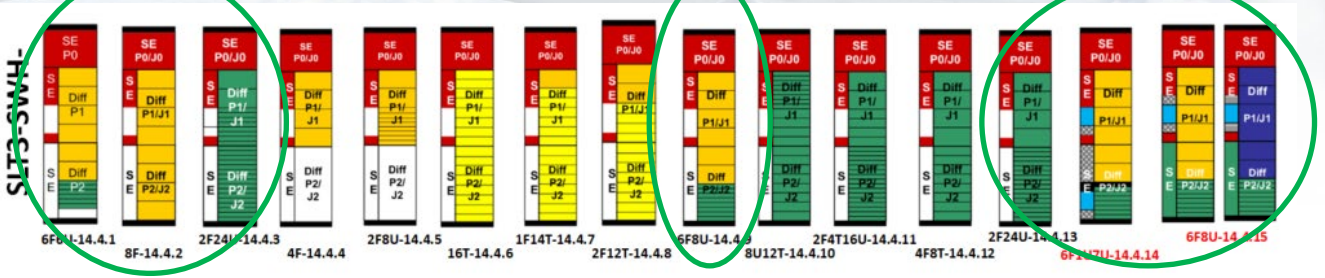
2017

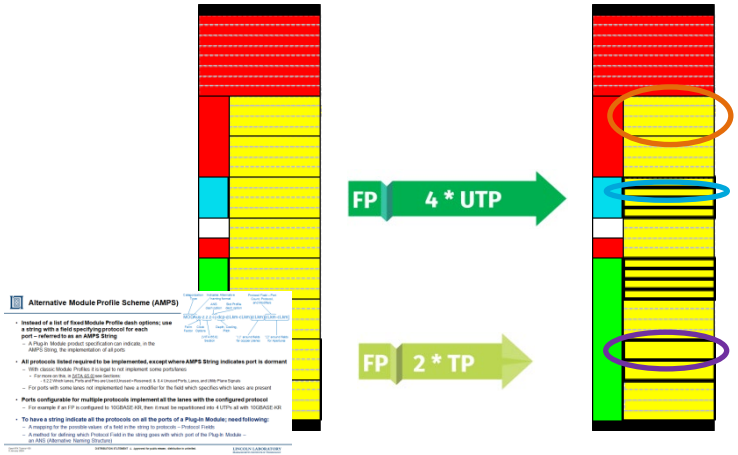
2019

2023

5.1 Ethernet
- 5.1.1 1000BASE-BX (1.25 Gbaud Signaling)
- 5.1.2 1000BASE-KX (1.25 Gbaud Signaling)
- 5.1.3 1000BASE-T (0.125 Gbaud Signaling)
- 5.1.4 10GBASE-BX4 (3.125 Gbaud Signaling)
- 5.1.5 10GBASE-KX4 (3.125 Gbaud Signaling)
- 5.1.6 10GBASE-T (0.800 Gbaud Signaling)
- 5.1.7 10GBASE-KR (10.3125 Gbaud Signaling)
- 5.1.8 40GBASE-KR4 (10.3125 Gbaud Signaling)
- 5.1.9 1000BASE-SX (1.25 Gbaud Signaling Over Optical Fiber)
- 5.1.10 10GBASE-LR (10.3125 Gbaud Signaling Over Single-Mode Optical Fiber)
- 5.1.11 10GBASE-SR (10.3125 Gbaud Signaling Over Multi-Mode Optical Fiber)
- 5.1.12 40GBASE-SR4 (10.3125 Gbaud Signaling Over Multi-Mode Optical Fiber)
- 5.1.13 100GBASE-SR10 (10.3125 Gbaud Signaling Over Multi-Mode Optical Fiber)
- 5.1.14 100BASE-TX (0.125 Gbaud Signaling)
- 5.1.15 25GBASE-KR (25.78125 Gbaud Signaling)
- 5.1.16 25GBASE-KR-S (25.78125 Gbaud Signaling)
- 5.1.17 25GBASE-SR (25.78125 Gbaud Signaling Over Multi-Mode Optical Fiber)
- 5.1.18 100GBASE-KR4 (25.78125 Gbaud Signaling)
- 5.1.19 100GBASE-SR4 (25.78125 Gbaud Signaling Over Multi-Mode Optical Fiber)
- 5.1.20 50GBASE-KR2 (25.78125 Gbaud Signaling)
- 5.1.21 50GBASE-SR2 (25.78125 Gbaud Signaling Over Multi-Mode Optical Fiber)
- 5.1.22 50GBASE-KR – (26.5625 Gbaud, PAM4 Signaling)
- 5.1.23 100GBASE-KR2 – (26.5625 Gbaud, PAM4 Signaling)
- 5.1.24 200GBASE-KR4 – (26.5625 Gbaud, PAM4 Signaling)
- 5.1.25 400GBASE-KR8 – (26.5625 Gbaud, PAM4 Signaling)

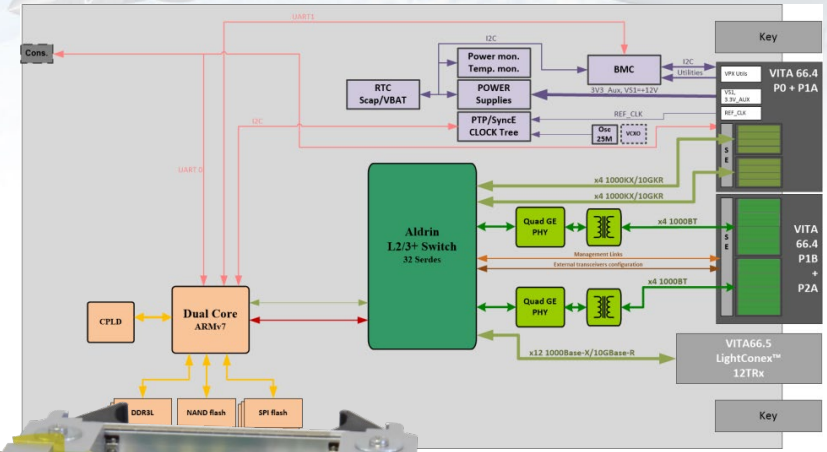
Switch Slots profiles Versatility

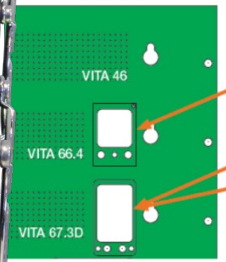




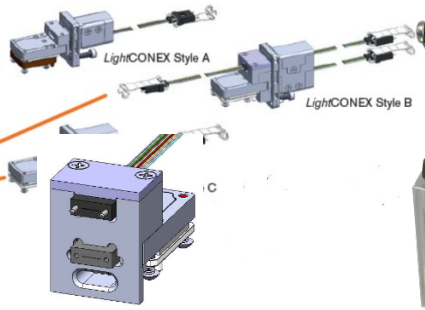
Refer to OpenVPX Tutorial and Common Practices
G. Rocco
Alternative Module Profile Scheme (AMPS)

Backplane Optical Interfaces

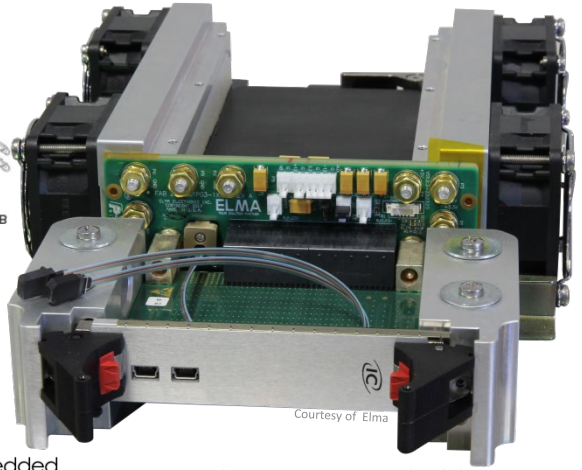




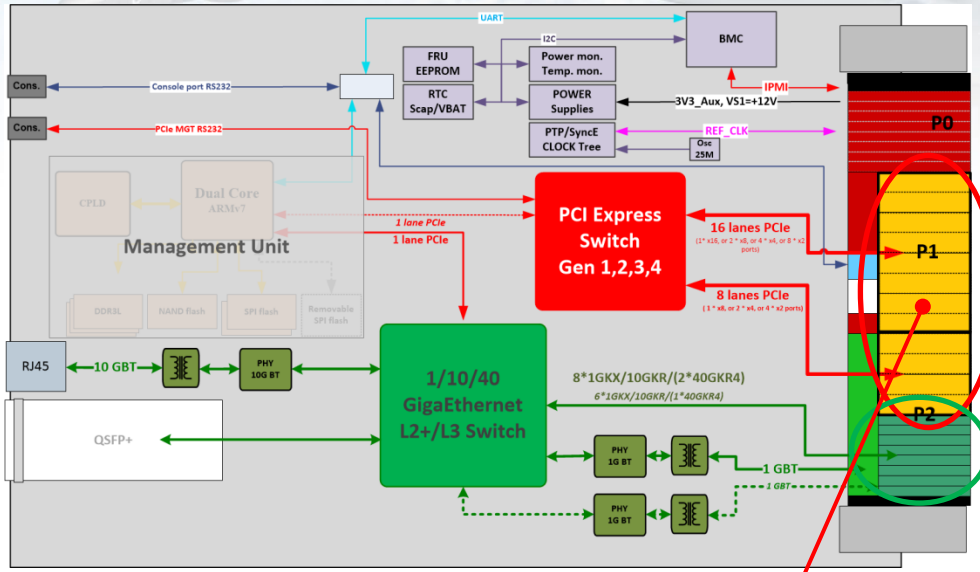
Source Reflex Photonics



Style-B
Active-Passive

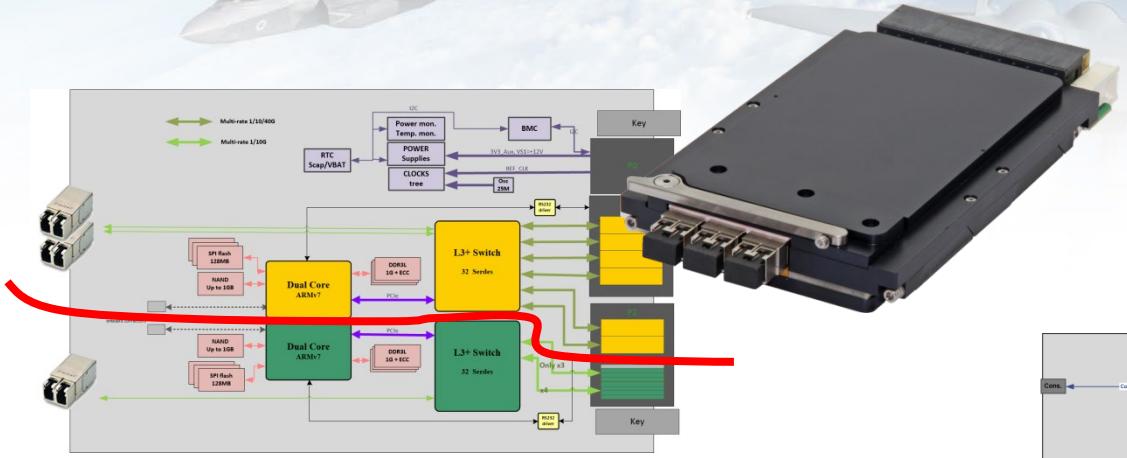


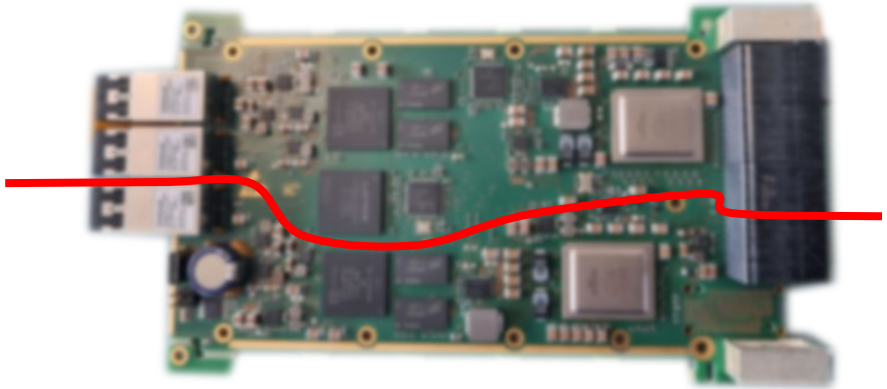
Dual Plane Hybrid Switch

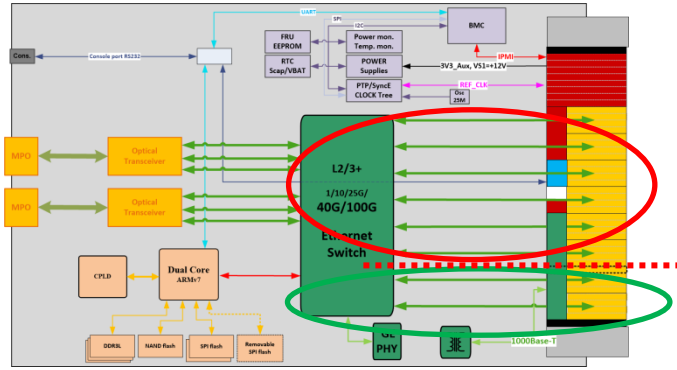


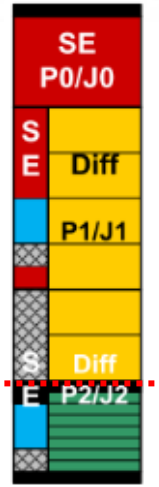
MOD3-SWH-6F8U-16.4.16-			DP01 - DP05, DS01 (FP)		CPutp01 - CPutp07	CSutp01	CPtp01
MOD3-SWH-6F8U-16.4.16- 1	2019-11	SLT3-SWH-6F8U-14.4.15	PCIe Gen 2 -- 5.3.3.2		1000BASE-KX -- 5.1.2	1000BASE-KX -- 5.1.2	1000BASE-T -- 5.1.3
MOD3-SWH-6F8U-16.4.16- 2	2019-11	SLT3-SWH-6F8U-14.4.15	PCIe Gen 3 -- 5.3.3.3		10GBASE-KR -- 5.1.7	10GBASE-KR -- 5.1.7	1000BASE-T -- 5.1.3
MODA3-16.4.16-	**STD Date**	**Slot Profile**	**Protocols for Copper Planes**				
MODA3-16.4.16- 1	2021-10	SLT3-SWH-6F8U-14.4.15	(FPs of DP01 - DP05, DS01	UTPs of DP01 - DP05, DS01)	(CPutp01 - CPutp07, CSutp01		CPtp01)

Dual Plane (isolated) Ethernet Switch









Conclusion

Questions…

Thank you for your attention!